AMENDMENTS TO THE SPECIFICATION

Page 1, first heading:

BACKGROUND ~~OF THE INVENTION~~

Page 1, lines 7-12:

Technical Field ~~of the Invention~~

~~The present invention relates to a~~ A method ~~of~~ for forming an isolation layer in the semiconductor device is disclosed~~, and more particularly, to a method of forming an isolation layer in the semiconductor device~~, which is capable of simultaneously preventing a concentration of an electric field on ~~the~~ a top corner of a trench and formation of an undesirable moat.

Page 1, lines 15-23:

In all the processes of manufacturing semiconductor devices, an isolation layer is formed in an isolation region in order to electrically isolate respective devices formed at the semiconductor substrate. In the prior art, the isolation layer is formed by LOCOS (local oxidation) process. ~~At~~ As the degree of integration ~~in~~ of the semiconductor device increases, however, the isolation layer has recently been formed by means of a process of etching the semiconductor substrate by a given depth to form the trench and the trench is buried with an insulating material. The isolation layer formed thus is called a ~~trench type~~ trench-type isolation layer.

Page 1, line 24 to Page 2, line 10:

The ~~trench type~~ trench-type isolation layer is formed by forming a pad oxide film and a pad nitride film through which the isolation region is exposed on a semiconductor substrate, etching the semiconductor substrate in the isolation region and then burying an insulating material layer. Thus, even though the pad nitride film and the pad oxide film are removed, the insulating material layer buried between the pad nitride film and the pad oxide film remains intact. Due to this, the isolation layer consisting of the insulating material layer has a shape in which the isolation layer is buried into the trench and a shape in which the width of the isolation layer is ~~narrow~~ narrower than that of the isolation region and the upper side thereof is projected higher than the surface of the semiconductor substrate.

Page 2, lines 11-19:

~~Even in~~ In the ~~process of~~ manufacturing of flash memory cells, the isolation layer is also formed using the trench type isolation layer. ~~At this time,~~ Currently, the isolation layer is formed by means of SAFG (self aligned floating gate) process by which a polysilicon layer for a floating gate is isolated by a projection of the ~~trench type~~ trench-type isolation layer. If the polysilicon layer for the floating gate is isolated by the projection of the ~~trench type~~ trench-type isolation layer, a region where the floating gate will be formed can be ~~secured by maximum~~ reduced since the distance between the floating gates can be more narrowed. Therefore, the coupling ratio of the floating gate ~~could~~ can be increased.

Page 2, line 20 to Page 3, line 1:

In the above process, one of the most important things ~~is~~ to prevent ~~that~~ is the tunnel oxide film or the gate oxide film ~~is thinly formed~~ from being too thin, while simultaneously preventing a concentration of the electric field at a top corner of the trench and the formation of a moat~~, using the top corner slope of the trench~~. There is a problem in that the top corner of the trench may not be formed locally within the wafer ~~since~~ because the process conditions of the etch process for forming the isolation layer ~~is varied~~ can vary.

Page 3, line 3 to Page 5, line 16:

SUMMARY OF THE ~~INVENTION~~ DISCLOSURE

Accordingly, ~~the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art, and an object of the present invention is to provide~~ a method ~~of~~ for forming an isolation layer in ~~the~~ a semiconductor device~~,~~ is disclosed which is capable of simultaneously preventing a concentration of the electric field and formation of a moat.~~,~~ ~~by forming~~ The disclosed method forms the isolating film by ~~means of a method in which a method of~~ forming a ~~V type~~ V-type trench at the isolation region, implanting ions capable of accelerating oxidization action into the center portion of the ~~V type~~ V-type trench, implementing an oxidization process to form an insulating film consisting of an oxide film at the isolation region, and then completely burying the trench with an insulating material, using the LOCOS method, and ~~a method of~~ forming a ~~trench type~~ trench-type isolation layer, ~~are applied together,~~ whereby ~~the~~ a top corner of the trench is formed with an inclination.

In ~~a preferred~~ an embodiment, the method ~~of forming the isolation layer in the semiconductor devices according to the present invention is characterized in that it~~ comprises ~~the steps of~~ sequentially forming a tunnel oxide film and a pad nitride film on a semiconductor substrate and then forming an aperture through which an isolation region of the semiconductor substrate is exposed, forming a ~~V type~~ V-type trench at the isolation region, forming an insulating film spacer at the sidewall of the pad nitride film in the aperture, forming an ion implantation layer for accelerating oxidization at the bottom of the ~~V type~~ V-type trench that is exposed through the aperture, forming a first insulating film at the ~~V type~~ V-type trench by means of an oxidization process, burying the aperture on the first insulating film with a second insulating film, and removing the pad nitride film and the pad oxide film.

In the above, a tilt angle of the ~~V type~~ V-type trench is in the range of 25 ~ 45°.

The ion implantation layer is formed by implanting arsenic (As). At this time, arsenic (As) is implanted with energy of 15 ~ 50keV and the dose of implantation of As is 1E14 ~ 1E16cm^{-2}.

The oxidization process is performed at a temperature of 800 ~ 950°C by setting an oxidization target thickness of 300 ~ 1000Å, whereby the first insulating film is formed ~~in~~ with a thickness in the range of 1500 ~ 4000Å by means of the ion implantation layer for accelerating oxidization.

The second insulating film is formed using a HDP oxide film and is formed ~~in~~ with thickness in the range of 2000 ~ 5000Å.

Additional advantages~~, objects,~~ and features of the ~~invention~~ disclosed methods will be set forth in part in the following detailed description ~~which follows and in part~~ other features and advantages will become apparent to those ~~having~~ of ordinary skill in the art upon examination of ~~the following or may be learned from practice of the invention~~ this disclosure. ~~The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.~~

~~In another aspect of the present invention, it is to~~ It will be understood that both the foregoing general description and the following detailed description ~~of the present~~

~~invention~~ are exemplary and explanatory and are intended to provide further explanation of the ~~invention as~~ methods claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other ~~objects,~~ features and advantages of the ~~present invention~~ disclosed methods will be apparent from the following detailed description ~~of the preferred embodiments of the invention~~ in conjunction with the accompanying drawings, ~~in which~~ wherein:

FIG. 1A through FIG. 1L are cross-sectional views of semiconductor devices for explaining a disclosed method of forming an isolation layer in the devices.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments ~~of the present invention~~, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

Page 6, lines 16 to Page 7, line 2:

Referring now to FIG. 1B, the pad nitride film **103** and the pad oxide film **102** are sequentially etched by means of etch process using the isolation mask (not shown), thus forming an aperture **104a** through which the isolation region of the semiconductor substrate **101** is exposed. Thereby, the pad oxide film **102** and the pad nitride film **103** through which the isolation region of the semiconductor substrate **101** is exposed are formed to be a stack structure.

Next, the semiconductor substrate **101** of the isolation region, which is exposed through the aperture **104a**, is etched to form a ~~V-type~~ V-type trench **104**. At this time, the etched portion of the pad nitride film **103** is formed to be vertical and the sidewalls of the V type trench **104** are formed to have a tilt angle of 25 ~ 45°.

Page 7, line 11 to Page 8, line 7:

Referring to FIG. 1D, the insulating material layer (**105a** in FIG. 1C) remains only at the sidewalls of the aperture **104a** in the pad nitride film **103**, by means of blanket

etch process, thus forming the insulating film spacer **105** at the sidewall of the pad nitride film **103**. While the width of the aperture **104a** is narrowed by the insulating film spacer **105**, only a deep portion at the center of the ~~V-type~~ V-type trench **104** is exposed.

By reference to FIG. 1E, in order to accelerate oxidization in a subsequent oxidization process, ions for accelerating oxidization are implanted into the deep portion of the center of the V type trench **104** exposed through the aperture **104a**. Thereby, an ion implantation layer **106** is formed at the deep portion of the center of the ~~V-type~~ V-type trench **104**.

In the above, the ion implanted into the deep portion of the center of the ~~V-type~~ V-type trench **104** may include arsenic (As). The dose of implantation is 1E14 ~ 1E16cm^{-2}. Meanwhile, when the ion is implanted by ion implantation process, the ion is implanted using the energy of 15 ~ 50keV.

Referring to FIG. 1F, in order to remove a native oxide film (not shown) formed on the surface of the ~~V-type~~ V-type trench **104**, the cleaning process is performed and a first insulating film **107** is then formed at the center of the ~~V-type~~ V-type trench (**104** in FIG. 1E) exposed through the aperture **104a**. At this time, the first insulating film **107** may be formed using an oxide film and the oxide film is formed by the oxidization process of a wet or dry oxidization mode.

Page 8, line 14 to Page 9, line 11:

By reference to FIG. 1G, after a second insulating film 108 is formed ~~on~~ in the ~~entire structure~~ trench, and, as shown in Fig. 1H, the second insulating film 108, insulating material 105 and ~~on~~ the pad nitride film **103** ~~is~~ are removed. At this time, the second insulating film 108 on the pad nitride film **103** may be removed by means of chemical mechanical polishing using the pad nitride film **103** as a polishing stop layer.

Meanwhile, after the pad nitride film **103** is completely removed in a subsequent process, the height of the isolation layer **109** that protrudes upwardly from the surface of the semiconductor substrate **101** may be determined depending on the original thickness of the pad nitride film **103** remaining after the chemical mechanical polishing. Therefore, if the top of the pad nitride film **103** is excessively removed as the second insulating film on the pad nitride film **103** is removed to expose the pad nitride film **103** during the chemical mechanical polishing process, the ~~height~~ extent of the projection of the isolation layer **109**

that ~~is protruded~~ protrudes higher than the surface of the semiconductor substrate is ~~lowered~~ reduced. This affects the height of the polysilicon layer for the floating gate to be formed in a subsequent process. Accordingly, it is preferred that the process conditions of the chemical mechanical polishing process ~~is~~ be controlled so that the projected top of the isolation layer **109** is not lowered.

Thereby, the isolation layer **109** which consists of the ~~having a~~ second insulating film **108** remaining only at the aperture **104a** on ~~a~~ the first insulating film **107** and ~~consisting of the first and second insulating films **107 and 108,**~~ is formed.

Page 9, line 21 to Page 10, line 2:

Through the above processes, the isolation layer 109 ~~of the present invention~~ is formed. Thereafter, if a flash memory cell is to be manufactured, the pad nitride film 103 and the pad oxide film 102 are removed, and the tunnel oxide film, the floating gate the dielectric film and the control gate are then formed on the semiconductor substrate. This manufacture process will be below described in short.

Page 10, lines 16-22:

At this time, in the process of removing the pad oxide film (**102** in FIG. 1H), the projection **109a** of the isolation layer **109** is also etched by a given thickness. The top of the projection **109a** of the isolation layer **109** is wider than the bottom thereof. In the process of removing the pad oxide film (**102** in FIG. 1H), however, the top of the projection **109a** is more etched than the bottom thereof, so that the difference in widths of the top and bottom of the projection **109a** ~~become similar~~ is reduced.

Page 11, line 9 to Page 12, line 4:

Meanwhile, the tunnel oxide film **111** is formed by the wet oxidization process at a temperature of 750 ~ 800°C. Next, the tunnel oxide film **111** is annealed under nitrogen atmosphere at a temperature of 900 ~ 910°C for 20 ~ 30 minutes, thus minimizing the interfacial defect intensity of the semiconductor substrate **101** and the tunnel oxide film **111**. Further, the first polysilicon layer **112** for forming the floating gate is formed using a highly doped polysilicon layer. ~~into which an impurity of a high concentration is doped. Explaining in more detail,~~ Specifically, the first polysilicon layer **112** is formed by means of

a LP-CVD (low pressure chemical vapor deposition) method using one of SiH_4 or Si_2H_6 and PH_3 gas as a source ~~so that~~ with an impurity of 1.5E20 ~ 3.0E20 atoms/cc ~~is doped~~. Further, the first polysilicon layer **112** is formed at a temperature of 580 ~ 620°C under a low pressure condition of 0.1 ~ 3Torr in order to minimize the grain size so that the electric field is not concentrated at one place. The first polysilicon layer **112** is formed in thickness of 800 ~ 2000Å.

Further, the chemical mechanical polishing process is implemented so that the first polysilicon layer **112** can be completely isolated by the projection **109a** using the projection **109a** of the isolation layer **109** as an etch stop layer. Preferably, the chemical mechanical polishing process is performed so that the first polysilicon layer **112** remains ~~in~~ at a thickness in the range of 800 ~ 1400Å.

Referring to FIG. 1K, the projection (**109a** in FIG. 1J) of the isolation layer **109**) that is exposed between the first polysilicon layers **112** is removed using HF or BOE (buffered oxide etchant). Thereby, the lateral sides of the first polysilicon layer **112** for the floating gate, which contacts the projection **109a** in FIG. 1J) of the isolation layer **109**, ~~is~~ are exposed, so that the coupling ratio of the floating gate ~~could~~ can be increased.

Page 12, line 18 to Page 13, line 13:

At this time, lower and upper oxide films of the ONO dielectric film 113 may be formed using a HTO (hot temperature oxide) film, which is formed using DCS (SiH_2Cl_2) and N_2O gas having a good internal pressure and a good TDDB (time dependent dielectric breakdown) characteristic gas as a source gas. Further, the silicon nitride film is formed by means of the LP-CVD method using DCS (SiH_2Cl_2) and NH_3 gas at a temperature of 650 ~ 800°C and at a low pressure of 1 ~ 3Torr. After the dielectric film **113** of the ONO structure is formed, a steam anneal process may be performed in a wet oxidization mode at a temperature of 750 ~ 800°C in order to improve the interfacial characteristic between the films. The steam anneal process is performed so that an oxidization target thickness is in the range of 150 ~ 300Å on bare Silicon wafer (monitoring wafer) base.

Meanwhile, the lower oxide film, the silicon nitride film and the upper ~~nitride~~ oxide film are deposited in thickness corresponding to their device characteristics, wherein respective processes of depositing the oxides proceed with no time delay in order to prevent contamination of them with the native oxide film or impurities. At this time, it is preferred

that the lower oxide film is formed in thickness of 35 ~ 60Å, the silicon nitride film is formed in thickness of 50 ~ 65Å and the upper oxide film is formed in thickness of 35 ~ 60Å.

Page 14, line 1-14:

As described above, the disclosed methods of manufacturing the flash memory cell ~~according to the present invention~~ can have the following advantages.

First, only one isolation mask for defining an isolation region is used in the process of forming the isolation layer. Accordingly, the degree of difficulty in the process can be lowered and the process cost ~~could~~ can be reduced.

Second, the top corner of the trench is formed ~~to have~~ with a small tilt angle ~~of a low angle~~. It is thus possible to prevent the tunnel oxide film or the gate oxide film form being too thinly formed in a subsequent process and is possible to prohibit the unwanted generation of a moat structure.

Third, the polysilicon layer for the floating gate is isolated by means of the projection of the isolation layer and the projection is then removed to increase the coupling ratio. Thus, the critical dimension can be minimized to form a uniform floating gate and variation in the coupling ratio ~~could~~ can be prevented.

Page 14, line 22 to page 18 line 14:

Sixth, the process margin can be secured and a high-integration flash memory cell of over 0.13um level ~~could~~ can be also easily manufactured, with the existing equipments and processes without using complex processes and expensive equipments.

The forgoing embodiments are merely exemplary and are not to be construed as limiting ~~the present invention~~ of this disclosure. The ~~present~~ teachings of this disclosure can be readily applied to other types of apparatuses. ~~The description of the present invention is intended to be illustrative, and not to limit the scope of the claims.~~ Many alternatives, modifications, and variations will be apparent to those skilled in the art.

Please amend the abstract as follows: